

09/901,079

RCE

Application No.: 09/901,079

Docket No.: 8733.464.00-US

Amendment dated April 14, 2004

Reply to final Office Action dated January 14, 2004

1, 2, 16, 30

Listing of the Claims:

1. (Currently Amended) An in-plane switching liquid crystal display device comprising:
first and second substrates;
a gate line arranged in one direction on the first substrate;
a common line arranged on the first substrate;
a gate insulation layer on the first substrate;
a data line on the gate insulation layer;
a first passivation layer on the gate insulation layer;
a plurality of common electrodes in contact with [[on]] the first passivation layer;
a second passivation layer on the first passivation layer, wherein the second passivation layer is an inorganic material;
a plurality of pixel electrodes on the second passivation layer; and
a liquid crystal layer between the first and second substrates.
2. (Currently Amended) The device of claim 1, wherein the common and pixel electrodes are formed of [[the]] a transparent conductive material.
3. (Original) The device of claim 2, wherein the transparent conductive material includes at least one of indium tin oxide (ITO) or indium zinc oxide (IZO).
4. (Original) The device of claim 1, wherein the gate insulation layer and the second passivation layer are one of Silicon Nitride (SiN_x) and Silicon Oxide (SiO₂).
5. (Original) The device of claim 1, wherein the first passivation layer is formed of an organic material.
6. (Original) The device of claim 5, wherein the organic material is one of benzocyclobutene (BCB) and acryl.
7. (Original) The device of claim 1, wherein the common line is parallel with the gate line and spaced apart from the gate line.
8. (Original) The device of claim 1, wherein the data line is perpendicular to the gate line.

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9. (Previously Presented) The device of claim 1, further comprising a thin film transistor at a crossing point of the gate line and the data line.
10. (Original) The device of claim 9, wherein the thin film transistor includes a gate electrode, an active layer, and source and drain electrodes.
11. (Original) The device of claim 1, wherein the first passivation layer includes a plurality of common line contact holes.
12. (Previously Presented) The device of claim 11, wherein each common electrode is electrically connected with the common line through a corresponding common line contact hole.
13. (Original) The device of claim 1, wherein the second passivation layer includes a drain contact hole.
14. (Original) The device of claim 13, wherein one of the plurality of pixel electrodes is electrically connected with the drain electrode through the drain contact hole.
15. (Original) The device of claim 1, wherein each pixel electrode is arranged between the adjacent common electrodes.
16. (Currently Amended) A method of fabricating an array substrate for an in-plane switching liquid crystal device, the method comprising:
 - forming a gate electrode, a gate line and a common line on a substrate with a first metal layer;
 - forming a gate insulation layer on the substrate;
 - forming a data line and source and drain electrodes with a second metal layer;
 - forming a first passivation layer on the gate insulation layer;
 - forming a plurality of common electrodes in contact with [[on]] the first passivation layer;
 - forming a second passivation layer on the first passivation layer, wherein the second passivation layer is an inorganic material; and
 - forming a plurality of pixel electrodes on the second passivation layer.

17. (Original) The method of claim 16, wherein the step of forming the plurality of common electrodes comprises depositing and patterning a first transparent conductive material.
18. (Original) The method of claim 17, wherein the first transparent conductive material is one of indium tin oxide (ITO) and indium zinc oxide (IZO).
19. (Original) The method of claim 16, wherein the step of forming the pixel electrodes comprises depositing and patterning a second transparent conductive material.
20. (Original) The method of claim 19, wherein the second transparent conductive material is one of indium tin oxide (ITO) and indium zinc oxide (IZO).
21. (Original) The method of claim 16, wherein the first passivation layer is an organic material.
22. (Original) The method of claim 21, wherein the organic material is one of benzocyclobutene (BCB) and acryl.
23. (Original) The method of claim 16, wherein the gate insulation layer and the second passivation layer are one of Silicon Nitride (SiN_x) and Silicon Oxide (SiO_2).
24. (Original) The method of claim 16, wherein the first and second metal layer include a material selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), antimony (Sb), and an alloy thereof.
25. (Original) The method of claim 16, wherein the first passivation layer includes a plurality of common line contact holes.
26. (Original) The method of claim 25, wherein each common electrode is electrically connected with the common line through each common line contact hole.
27. (Original) The method of claim 16, wherein the second passivation layer includes a drain contact hole.
28. (Original) The method of claim 27, wherein one of the plurality of pixel electrodes is electrically connected with the drain electrode through the drain contact hole.

29. (Original) The method of claim 16, wherein each pixel electrode is arranged between adjacent common electrodes.

30. (Currently Amended) An in-plane switching liquid crystal display device, comprising:
first and second substrates;
gate lines on the first substrate;
data lines perpendicular to the gate lines to form a plurality of pixel regions;
a thin film transistor in each of the pixel regions at a crossing point of the data lines and the gate lines;
a common line on the first substrate in each of the pixel regions, the common line parallel to the gate lines;
a first insulation layer over the gate lines, the data lines being on the first insulation layer;
a second insulation layer over the data lines and the common line;
a plurality of first contact holes through the first and second insulation layers over the common line;
a plurality of common electrodes in contact with [[on]] the second insulation layer, wherein the common electrodes contact the common line via the first contact holes;
a third insulation layer on the common electrodes and the second insulation layer, wherein the third insulation layer is an inorganic material;
a second contact hole through the second and third insulation layers over a drain electrode of the thin film transistor;
a plurality of pixel electrodes on the third insulation layer; and
a liquid crystal interposed between the first and second substrates.

31. (Original) The device of claim 30, wherein the pixel electrodes electrically communicate with one another via a transverse pixel electrode perpendicular to the common electrodes.

32. (Original) The device of claim 30, wherein the pixel electrodes and the common electrodes are formed of a transparent conductive material.

33. (Original) The device of claim 30, wherein the transparent conductive material is one of indium tin oxide and indium zinc oxide.

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34. (Original) The device of claim 30, wherein the first and third insulation layers are formed of one of Silicon Nitride (SiNx) and Silicon Oxide.

35. (Original) The device of claim 30, wherein the second insulation layer is formed of an organic material.

36. (Original) The device of claim 35, wherein the organic material is one of benzocyclobutene (BCB) and acryl.